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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/398,689	MRASEK, ARMIN	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-7* is/are allowed.

6)☒ Claim(s) *1-4,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 31st of January 2005. Claims 5 and 9 have been amended; no claim has been canceled; and no claim has been newly added since the RCE(2) Non-Final Office Action was mailed on 29th of September 2004. Currently, claims 1-9 are pending in this application.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [hereinafter AAPA] in view of Babin [US 5,506,747 A] and Willenz [US 5,841,722 A].

Referring to claim 1, AAPA discloses an improved ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable lengths from a first data bus to a second data bus operated asynchronously with respect to said first data bus and controlled by a microprocessor (See the preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*), said improvement which comprises: writing said digital data of a given HDLC-data frame (See page 1, lines 7-10 and 22-23; i.e., wherein in fact that digital data is divided up into data frames of variable length, and the HDLC protocol is used for the ISDN implies said digital data of a given HDLC-data frame) from said first data bus to a memory having a fixed size (See page 2, lines 10-11; i.e., wherein in fact that an output signal from the HDLC Receiver logic unit is supplied to a FIFO memory implies that said digital data is written from said first data bus to said memory); informing said microprocessor, in a form of an interrupt signal (i.e., interrupt Int; See page 9, line 25) generated by a memory control unit (i.e., HDLC Receiver/Transmitter), if said memory is full or

if said memory contains an entry indicating an end of a respective HDLC-data frame (See page 9, line 26 through page 10, line 1; i.e., wherein in fact that the HDLC Receiver always triggers an interrupt Int in the microprocessor if either the FIFO reception memory (viz., memory) is full or if the received D-channel signals (viz., a respective data frame) contain a byte indicating a frame end implies that informing said microprocessor, in a form of an interrupt signal generated by a memory control unit, if said memory (viz., FIFO reception memory) is full or if said memory contains an entry indicating an end of a respective HDLC-data frame (viz., a byte indicating a frame end of a respective data frame)); reading via said microprocessor said digital data from said memory (See page 2, lines 11-12; i.e., wherein in fact that a microprocessor removes the data contained in the FIFO memory implies that said microprocessor reads said digital data from said memory); and transmitting from said microprocessor to said memory control unit (i.e., HDLC Receiver/Transmitter) an acknowledgment of a reception of said data (viz., digital data) being read out from said memory (See Data signal and Ack signal from TP to HDLC Transmitter in Fig. 6A and B).

AAPA does not teach said memory being arranged directly between said first data bus and said second data bus, and having a settable size; and determining via said microprocessor from said memory control unit a quantity of said digital data to be read from said memory.

Babin discloses a provision of FIFO buffer in RAM (See Fig. 1 and Abstract), wherein a memory (i.e., RAM 10 of Fig. 1) being arranged directly between a first data bus (i.e., input path 18 of Fig. 1) and a second data bus (i.e., output path 20 of Fig. 1), and having a settable size (See col. 1, line 55 through col. 2, line 15); and determining via a microprocessor (i.e., under the control of processor; See col. 3, lines 14-16) from a memory control unit (i.e., processor and store 12 in Fig. 1) a quantity of digital data (i.e., pseudo frame count) to be read from said memory (See col. 3, lines 16-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of addressing arrangement for said memory, as disclosed by Babin, in

said method for transmitting digital data, as disclosed by AAPA, for the advantage of providing many FIFOs of variable sizes (See Babin, col. 1, lines 5-8).

AAPA, as modified by Babin, does not teach setting dynamically via said microprocessor a size of said memory for a current reading/writing procedure of said memory.

Willenz discloses a variable sized FIFO buffer (See Fig. 1 and Abstract), wherein setting dynamically via a microprocessor (i.e., controller 16 of Figs. 1 and 2) a size of a memory (i.e., a variable size of FIFO buffer, viz., upper FIFO 10, lower FIFO, 12 and Random Access Memory 14 in Fig. 1) for a current reading/writing procedure of said memory (See col. 1, lines 26-29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said controller for said dynamic setting of said memory, as disclosed by Willenz, in said memory controller, as disclosed by AAPA, as modified by Babin, for the advantage of providing an improved memory (i.e., FIFO buffer) for buffering data between said first data bus and said second data bus (in fact, two systems; See Willenz, col. 1, lines 23-25).

Referring to claim 2, AAPA teaches supplying said digital data from said first data bus (See Fig. 6A and 6B) to a high-level data link control logic unit (i.e., HDLC control device; See page 2, lines 7-8) which checks whether said digital data has been received correctly (See page 1, line 25 through page 2, line 1 and lines 7-9; i.e., wherein in fact HDLC control device checks the data protection information implies that said HDLC logic unit checks whether said digital data has been received correctly) before said digital data is written to said memory (See page 2, lines 7-8; i.e., wherein in fact that an incoming D-channel signal is supplied to an HDLC Receiver logic unit implies that said digital data (i.e., HDLC signal) has been received before said digital data is written to said memory).

Referring to claim 8, AAPA teaches said memory comprises a FIFO (See page 2, lines 10-11).

4. Claims 3, 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Babin [US 5,506,747 A], Willenz [US 5,841,722 A] and Chee et al [US 5,673,416; hereinafter Chee].

Referring to claim 3, AAPA discloses an improved ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable lengths from a first data bus, controlled by a microprocessor, to a second data bus operated asynchronously with respect to said first data bus (See the preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*), said improvement which comprises: writing said digital data from said first data bus to a memory having a fixed size (See page 2, lines 10-11; i.e., wherein in fact that an output signal from the HDLC Receiver logic unit is supplied to a FIFO memory implies that said digital data is written from said first data bus to said memory); informing said microprocessor, in a form of an interrupt (See page 9, line 25) generated by a memory control unit (i.e., HDLC Receiver/Transmitter), if said memory is full or an end of a data frame has been reached (See page 9, line 26 through page 10, line 1); and transmitting from said microprocessor to said memory control unit (i.e., HDLC Receiver/Transmitter) an acknowledgment of said data being written into said memory (See Data signal and Ack signal from TP to HDLC Receiver in Fig. 6A and B).

AAPA does not teach said memory being arranged directly between said first data bus and said second data bus, and having a settable size.

Babin discloses a provision of FIFO buffer in RAM (See Fig. 1 and Abstract), wherein a memory (i.e., RAM 10 of Fig. 1) being arranged directly between a first data bus (i.e., input path 18 of Fig. 1) and a second data bus (i.e., output path 20 of Fig. 1), and having a settable size (See col. 1, line 55 through col. 2, line 15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of addressing arrangement for said memory, as disclosed by Babin, in said method for transmitting digital data, as disclosed by AAPA, for the advantage of providing many FIFOs of variable sizes (See Babin, col. 1, lines 5-8).

AAPA, as modified by Babin, does not teach setting dynamically via said microprocessor a size of said memory for a following reading/writing procedure of said memory, said settable size being dependent on said size of said transmitted HDLC-data frame being written at the same time in said memory.

Willenz discloses a variable sized FIFO buffer (See Fig. 1 and Abstract), wherein setting dynamically via a microprocessor (i.e., controller 16 of Figs. 1 and 2) a size of a memory (i.e., a variable size of FIFO buffer, viz., upper FIFO 10, lower FIFO, 12 and Random Access Memory 14 in Fig. 1) for a following reading/writing procedure of said memory (See col. 1, lines 26-29), said settable size (i.e., value of write counter 38 of Fig. 1) being dependent on a size of a transmitted HDLC-data frame being written at the same time in said memory (See col. 3, line 16 through col. 4, line 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said controller for said dynamic setting of said memory, as disclosed by Willenz, in said memory controller, as disclosed by AAPA, as modified by Babin, for the advantage of providing an improved memory (i.e., FIFO buffer) for buffering data between said first data bus and said second data bus (in fact, two systems; See Willenz, col. 1, lines 23-25).

AAPA, as modified by Babin and Willenz, does not teach performing one of informing said microprocessor, in a form of said interrupt generated by said memory control unit, if said memory is ready to accept new data from said first data bus, and said microprocessor asking said memory control unit if said memory is ready to accept said new data from said first data bus; and writing via said microprocessor said new data to said memory.

Chee discloses a memory request and control unit (See Abstract), wherein performing one of informing a microprocessor (i.e., display FIFO module 12 of Fig. 2), in a form of interrupt (i.e., DispDataAck from DRAM controller sequencer 22 to display FIFO module 12 in Fig. 3) generated by a memory control unit (i.e., DRAM controller sequencer 22 of Fig. 3), if a memory (i.e., DRAM 24 of Fig. 3) is ready to accept new data (See col. 9, lines 20-23), and said microprocessor (i.e., display FIFO module) asking (i.e., a low

priority request DispLoReq in Fig. 3) said memory control unit (i.e., DRAM controller sequencer) if said memory is ready to accept said new data. (See col. 10, lines 55-57); writing via said microprocessor said new data to said memory (See col. 9, lines 58-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of memory request and control unit, as disclosed by Chee, in said method, as disclosed by AAPA, as modified by Babin and Willenz, for the advantage of utilizing simple circuit for said microprocessor (i.e., display FIFO module) for efficiently determining when to issue requests for said memory (i.e., DRAM access; See Chee, col. 2, lines 41-43).

Thus, AAPA, as modified by Babin, Willenz and Chee, suggests placing said new data onto said second data bus (i.e., transmitting digital data (i.e., new data) to a second data bus; See the preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*).

Referring to claim 4, AAPA discloses supplying said new data (See Fig. 6A and 6B) to a high-level data link control logic unit (i.e., HDLC control device; See page 2, lines 7-8) before it is placed onto the second data bus (See page 2, lines 7-8; i.e., wherein in fact that an incoming D-channel signal is supplied to an HDLC Receiver logic unit implies that supplying said new data (i.e., HDLC signal) to a high-level data link control logic unit before it is placed onto the second data bus), said high-level data link control logic unit adding error-checking data (i.e., adding protection information) to said new data (See page 2, lines 16-18).

Referring to claim 9, AAPA teaches said memory comprises a FIFO (See page 2, lines 10-11).

Allowable Subject Matter

5. Claims 5-7 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 5, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that said second register has a content selectively modifiable with each read cycle of said microprocessor. The claims 6 and 7 are dependent claims of the claim 5.

Response to Arguments

7. Applicant's arguments filed on 31st of January 2005 (hereinafter the Response) have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "... In failing to teach a memory having a settable size, the AAPA not only fails to teach Applicant's particularly claimed memory (point 1: above), but in so lacking such a teaching, cannot even be found to suggest Applicant's claimed invention where the size of the memory is dynamically set in accordance with contemporaneously sent data (point 2: above). ..." on the Response page 8, line 12 through page 11, line 20, the Examiner believes that the Applicant misinterprets the claim rejection.

The Applicant essentially argues that AAPA doesn't teach the above argued elements. However, Babin suggests the claimed subject matter "a memory (i.e., RAM 10 of Fig. 1) being arranged directly between a first data bus (i.e., input path 18 of Fig. 1) and a second data bus (i.e., output path 20 of Fig. 1), and having a settable size (See col. 1, line 55 through col. 2, line 15)", and Willenz suggests the claimed limitations "setting dynamically via a microprocessor (i.e., controller 16 of Figs. 1 and 2) a size of said memory (i.e., a variable size of FIFO buffer, viz., upper FIFO 10, lower FIFO, 12 and Random Access Memory 14 in Fig. 1) for a current reading/writing procedure of said memory (See col. 1, lines 26-29)". Therefore, the combination of the references AAPA, Babin and Willenz with rationale suggests an obviousness of the claimed invention.

Furthermore, the Examiner emphasizes that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642

F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "In addition to the above elements of Applicant's claims missing from the AAPA, the AAPA additionally fails to teach or suggest other elements of Applicant's claimed invention, such as the 'informing' step of claim 1 and the reading of data, via the microprocessor. With regard to the reading of data of Applicant's claim 1, the AAPA only discloses a 'removal' of the data stored in the memory. However, the process of removal is neither identical to, nor equivalent to the process of reading. In fact, the process of removal is rather identical to the process of writing since the removal means that the respective memory portions are being written with a predefined logical value (i.e., '0') or an undefined state (i.e., 'floating'). In the removal process of the AAPA, the data to be removed form the memory are never read out before. In summary, since the process of removal is not the same as the process of reading, as required by Applicant's claim 1, this feature is not disclosed in the AAPA. Nor does the AAPA perform Applicant's informing step of claim 1. ..." on the Response page 11, line 21 through page 12, line 17, the Examiner respectfully disagrees.

First of all, in contrary to the Applicant's statement, AAPA suggests the claimed limitations "informing said microprocessor, in a form of an interrupt signal (i.e., interrupt Int; See page 9, line 25) generated by a memory control unit (i.e., HDLC Receiver/Transmitter), if said memory is full or if said memory contains an entry indicating an end of a respective HDLC-data frame (See page 9, line 26 through page 10, line 1; i.e., wherein in fact that the HDLC Receiver always triggers an interrupt Int in the microprocessor if either the FIFO reception memory (viz., memory) is full or if the received D-channel signals (viz., a respective data frame) contain a byte indicating a frame end implies that informing said microprocessor, in a form of an interrupt signal generated by a memory control unit, if said memory (viz., FIFO reception memory) is full or if said memory contains an entry indicating an end of a respective HDLC-data frame

(viz., a byte indicating a frame end of a respective data frame))", and "reading via said microprocessor said digital data from said memory (See page 2, lines 11-12; i.e., wherein in fact that a microprocessor removes the data contained in the FIFO memory implies that said microprocessor reads said digital data from said memory)". See paragraph 3 of the instant Office Action, claims 1, 2 and 8 rejection under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Babin and Willenz.

Secondly, with regard to the reading of data of Applicant's claim 1, the AAPA clearly teaches a 'removal' of the data stored in the memory, which is clearly suggesting the claimed process of reading. In other words, the 'removal' of the data stored in the FIFO memory clearly means the 'reading' of the data stored in the memory, which is supported by the AAPA on page 2, lines 13-18.

Furthermore, even though the Applicant asserts the process of "removal" of AAPA is rather identical to the process of writing since the removal means that the respective memory portions are being written with a predefined logical value (i.e., '0') or an undefined state (i.e., 'floating'), AAPA is silent on the Applicant's assertion, i.e., the removal means that the respective memory portions are being written with a predefined logical value (i.e., '0') or an undefined state (i.e., 'floating').

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "...Having a plurality of FIFOs of different sizes in a RAM, is not the same as dynamically sizing a memory in accordance with contemporaneously transmitted data, as is required by Applicant's claims. The size of the FIFOs in BAIN are preset, and the RAM is pre-informed of the 'depth' of each FIFO. ... In BAIN, the memory size is not set dynamically, as required by Applicant's claims. This is supported in the Office Action, on page 5, lines 1-2, which states ..." on the Response page 12, line 18 through page 13, line 25, the Examiner believes that the Applicant misinterprets the claim rejection.

The Applicant essentially argues that AAPA and Bain don't teach the above argued elements. Actually, the Examiner also admitted that AAPA, as modified by Bain, does not teach the above argued elements in

the prior/instant Office Actions. However, Willenz suggests the claimed subject matter "a variable sized FIFO buffer (See Fig. 1 and Abstract), wherein setting dynamically via a microprocessor (i.e., controller 16 of Figs. 1 and 2) a size of a memory (i.e., a variable size of FIFO buffer, viz., upper FIFO 10, lower FIFO, 12 and Random Access Memory 14 in Fig. 1) for a current reading/writing procedure of said memory (See col. 1, lines 26-29)".

Therefore, the combination of the references AAPA, Babin and Willenz with rationale suggests an obviousness of the claimed invention.

Furthermore, the Examiner emphasizes that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "... Applicant respectfully disagrees with the above statement of what is allegedly taught by WILLENZ. Although WILLENZ states that it discloses a 'variable sized' FIFO, it is not truly a 'memory having a settable size' as claimed by Applicant. ... However, neither the upper FIFO buffer, nor the lower FIFO buffer, nor the RAM of WILLENZ have a settable size, as required by Applicant's claims. As such, the WILLENZ reference fails to teach a memory 'having a settable size', as required by Applicant's claims. Further, WILLENZ fails to teach or suggest that its so-called 'variable-size' FIFO arrangement (the fixed size upper and lower FIFOs and RAM) has a size that is being dynamically set contemporaneously in accordance with the size of the data. ... WILLENZ fails to teach or suggest a memory having a settable size, and dynamically changing the size of a settable memory during the data communication (see claim 1 'for a current reading/writing procedure'; and claims 3 and 5 'written at the same time'), as claimed by Applicant." on the Response

page 13, line 26 through page 16, line 11, the Examiner believes that the Applicant misinterprets the claim rejection.

The Applicant essentially argues that Willenz doesn't teach the above argued elements, i.e., a memory having a settable size, and dynamically changing the size of a settable memory during the data communication. However, the combination of AAPA and Bain clearly suggests the claimed subject matter "a memory having a settable size", and in contrary to the Applicant's statement, Willenz teaches dynamically changing the size of a settable memory during the data communication, such that a variable sized FIFO buffer (See Willenz, Fig. 1 and Abstract), wherein setting dynamically via a controller 16 of Figs. 1 and 2 (i.e., microprocessor) a variable size of FIFO buffer, viz., upper FIFO 10, lower FIFO, 12 and Random Access Memory 14 in Fig. 1 (i.e., a size of a memory) for a current reading/writing procedure of said FIFO buffer (i.e., memory; See Willenz, col. 1, lines 26-29).

Therefore, the combination of the references AAPA, Babin and Willenz with rationale suggests an obviousness of the claimed invention.

Furthermore, the Examiner emphasizes that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Additionally, the CHEE reference was cited in the Office Action on page last paragraph, as allegedly disclosing a memory request and control unit. Even if, arguendo, CHEE were to teach the things alleged in the Office Action, CHEE neither teaches, nor suggests, a memory having a settable size, the size of which is set dynamically in accordance with contemporaneously transmitted data. As such, the CHEE reference cannot supply the missing

elements that are taught, nor suggested, in the AAPA, BAIN and WILLENZ references." on the Response page 16, lines 12-21, the Examiner believes that the Applicant misinterprets the claim rejection.

The Applicant essentially argues that Chee doesn't teach the above argued elements, i.e., a memory having a settable size, and dynamically changing the size of a settable memory during the data communication. However, the combination of AAPA, Bain and Willenz clearly suggests the claimed subject matter "a memory having a settable size, and dynamically changing the size of a settable memory during the data communication". See paragraph 4 of the instant Office Action, claims 3, 4 and 9 rejection under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Babin, Willenz and Chee.

Therefore, the combination of the references AAPA, Babin, Willenz and Chee with rationale suggests an obviousness of the claimed invention.

Furthermore, the Examiner emphasizes that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Thus, the Applicant's argument on this point is not persuasive.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Miller [US 5,915,104 A] discloses high bandwidth PCI to packet switched router bridge having minimized memory latency.

O'Brien [US 5,796,961 A] discloses heuristic bus access arbiter.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing

date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

cel/ CEL

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100